High-Order Inductorless Elliptic Filter with Reduced Number of Capacitors Using Signal-Flow Graphs

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Abstract—In this paper a method of realizing seventh-order elliptic filter using signal-flow graphs is presented. The elliptic filter having a minimum number of capacitors is compared with the filter having a higher number of capacitors. The version with minimum number of capacitors provides area savings in IC form. Both filters (i.e. filter with minimum and one with higher number of capacitors) have a low sensitivity to component tolerances in the pass band according to Orchard’s theorem. The seventh-order elliptic filter has three parallel capacitors forming three parallel tanks, and therefore has three finite elliptic transfer-function zeros. The realizations of one and two parallel capacitors have already been presented elsewhere. The sfg derivations necessary to realize seventh-order filter having additional resistive network is presented, which is very complicated in the case of three zeros. Transfer function magnitudes are simulated using the PSpice program. Monte Carlo runs confirm the low sensitivity to component tolerances of both circuit types.

Keywords: Seventh-order elliptic filters, IC design, signal-flow graphs, small chip area, low sensitivity.

I. INTRODUCTION

This paper presents a method in that signal-flow graph (sfg) derivations are applied to the passive-LCR ladder filters, in order to derive active-RC filter circuits. In recent paper [1] the method was applied to the elliptic filters of low order (up to sixth order), whereas in this paper high-order (i.e. seventh-order) elliptic filter is derived. The active-RC filters obtained by this method have a low sensitivity to component tolerances according to Orchard’s theorem, because they simulate passive-LCR ladder filter terminated with equal resistors in both ends [2]. When compared to allpole case, elliptic filters have additional capacitors to form finite zeros in transfer function. These zeros are realized by parallel LC tanks in series branches of ladder network. There are two main approaches how to realize those additional capacitors in the inductorless version of the filter (i.e. which is obtained by the simulation of passive-LCR ladder filter using signal-flow graphs). Two approaches are: (i) the filter with additional capacitive network (common approach), (ii) the filter with additional resistive network (new approach presented in this paper and in [1]). It will be confirmed by Monte Carlo runs using Cadence PSpice 16 [3] that both circuit types have low sensitivity to component tolerances.

Resistors are preferred over capacitors on a chip because they use less chip area and are easier to manufacture. The design method illustrated in [1] is for the case of low-order elliptic filters having one or two additional capacitors. In this paper the method is extended to the high-order filter having three capacitors. A systematic way is presented in which signal-flow graph is transformed to construct elliptic filter with canonic number of capacitors.

II. ELLIPTIC FILTERS WITH THREE TANK CAPACITORS

Consider the doubly terminated seventh-order low-pass elliptic passive-LCR ladder filter in Fig. 1(a) (as in [4][5]).

With Kirchhoff’s laws and the voltage-current branch relations of the passive-LCR ladder filter in Fig. 1(a), we obtain the set of equations:

\[
\begin{align*}
I_1 &= \frac{1}{R_s}(V_s - V_1), \\
V_1 &= \frac{1}{sC_1}(I_5 - I_2), \\
I_2 &= \left(\frac{1}{sL_2 + sC_2}\right)(V_1 - V_3), \\
V_3 &= \frac{1}{sC_3}(I_2 - I_4), \\
I_4 &= \left(\frac{1}{sL_4 + sC_4}\right)(V_3 - V_5), \\
V_5 &= \frac{1}{sC_5}(I_4 - I_6), \\
I_6 &= \left(\frac{1}{sL_6 + sC_6}\right)(V_5 - V_7), \\
V_7 &= \frac{1}{sC_7}(I_6 - I_8), \\
I_8 &= \frac{1}{R_i}V_{out}, \\
V_{out} &= V_7.
\end{align*}
\] (1)
Note that:

\[ I_2 = I_{C2} + I_{C2'}, \quad I_4 = I_{L4} + I_{C4}, \quad I_6 = I_{L6} + I_{C6}. \]  

(2)

Reformulating the system of equations (1) in order to obtain an appropriate sfg representation, we obtain:

\[
\begin{align*}
I_s &= \frac{1}{R_3} (V_3 - V_i), \\
V_i &= \frac{1}{C_i} (I_s - I_{L2}) + \frac{C_2}{C_i} V_3, \\
I_{L2} &= \frac{1}{sL_2} (V_i - V_j), \\
V_3 &= \frac{1}{sC_3} (I_{L2} - I_{L4}) + \frac{C_4}{C_3} V_3 + \frac{C_6}{C_3} V_5, \\
I_{L4} &= \frac{1}{sL_4} (V_3 - V_7), \\
V_5 &= \frac{1}{sC_5} (I_{L4} - I_{L6}) + \frac{C_7}{C_5} V_7, \\
I_{L6} &= \frac{1}{sL_6} (V_5 - V_8), \\
V_7 &= \frac{1}{sC_7} (I_{L6} - I_{L8}) + \frac{C_9}{C_7} V_7, \\
I_8 &= \frac{1}{R_8} V_{out}, \\
V_{out} &= V_i.
\end{align*}
\]

(3)

where

\[
\begin{align*}
C_1' &= C_1 + C_2, \\
C_3' &= C_3 + C_4, \\
C_4' &= C_4 + C_5 + C_6, \\
C_5' &= C_5 + C_7.
\end{align*}
\]

(4)

The sfg in Fig. 1(b) represents the system of equations (3).

In order to obtain voltage transfer functions for the paths of the sfg it is necessary to multiply the current nodes [e.g. in Fig. 1(b)] by a resistance, [e.g. R_0 [\Omega] in Fig. 2(a)]. As already shown in [1] and repeated here multiplying a node by some factor (the resistor R_0 in our case) means that all outgoing paths from this node will be multiplied by that factor. Thus, all incoming paths to that same node must be divided by the same factor. This is shown for the sfg in Fig. 1(b), and results in Fig. 2(a) and Fig. 2(b). To obtain a one to one relationship between currents and voltages, we select a value of R_0=1\Omega.

Two possible realizations of elliptic filters having three parallel tanks with C_2, C_4 and C_6 can be obtained from the system of equations (3); they are shown by sfgs in Fig. 2(a) and Fig. 4(a), respectively. In what follows we compare the two circuits resulting from these two sfgs with regard to complexity (number of resistors, capacitors, and chip area), and sensitivity.

<table>
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<th>Type</th>
<th>R_0</th>
<th>C_1</th>
<th>L_2</th>
<th>C_3</th>
<th>L_4</th>
<th>C_5</th>
<th>L_6</th>
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<td>1.85021</td>
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<td>25</td>
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<td>0.61906</td>
<td>1.66398</td>
<td>0.96224</td>
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<td>1.14130</td>
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</tr>
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</table>

TABLE I. ELEMENT VALUES OF LADDER-LCR FILTER IN FIG. 1(a)

Note that:

\[
T(s) = \frac{V_{out}}{V_{in}} = \frac{0.004483 \cdot (s^2 + 1.76)}{(s + 0.3764) (s^2 + 0.5822s + 0.3953) \times (s^2 + 2.397)(s^2 + 6.50) \times (s^2 + 0.2918s + 0.8051)(s^2 + 0.08155s + 1.027)}.
\]

(5)

and the resulting normalized component values (all of which are available from filter design handbooks) are given in Table I.

A. Networks with Additional Capacitors

The conventional method of deriving elliptic filters with additional capacitors is given in [6] and [7]. For our example, the obtaining an active-RC filter from its sfg, in a conventional way, starts with Fig. 2(a). After multiplication by R_0 sfg has all voltage nodes as shown in Fig. 2(b). Note that some incoming branches, which perform addition of signals have gain –1; this will result in some negative components. To obtain all positive components, we have to further transform the sfg in Fig. 2(b). Appropriate nodes have to be multiplied, or scaled, by –1 [see Fig. 2(b)-(d)] which results in sfg in Fig. 2(e) having positive and negative integrators, and all positive incoming branches. After “loop reduction” rule was applied, final sfg in Fig. 2(f) is obtained.
This results in the active RC circuit of Fig. 3, which is an inductorless active-RC simulation of the passive-LCR ladder network in Fig. 1(a). It is important to note that the low sensitivity to component tolerances, which are a characteristic of LCR ladder filters (see [2]), are carried over to their active-RC equivalents.

In this paper, all derivations will be carried out on single-ended designs; the conversion to a fully differential balanced version is straightforward and presented in [1].

B. Networks with Additional Resistors and Fewer Capacitors

As shown in [1], a third- to sixth-order elliptic filter has one or two parallel LC tank(s), which means one or two additional capacitor(s) $C_2$ (and $C_3$) when compared to the allpole filter of the same order. Seventh-order elliptic filter presented in this paper has three additional capacitors $C_2$, $C_4$ and $C_6$. According to the initial sfg in Fig. 4(a) [it is the same sfg as in Fig. 1(b)], which is shown again in Fig 4(c) (with only voltage nodes) the simulation of these capacitors resulted in six additional branches in the sfg with transmissions $C_2/C_1$ (from $V_1$ to $V_3$), $C_2/C_1$ (from $V_1$ to $V_3$), $C_2/C_1$ (from $V_3$ to $V_5$), $C_2/C_1$ (from $V_3$ to $V_5$), $C_2/C_1$ (from $V_3$ to $V_5$), and $C_2/C_1$ (from $V_3$ to $V_5$).

In order to derive the new circuit with additional resistors and fewer capacitors, we note that $V_1$, $V_3$, $R_3$ and $V_5$ are output nodes (because they are voltage outputs of opamps), therefore signal addition at these nodes is not possible. Thus, a sfg transformation must be performed in order to bring those signals to input nodes of opamps, where addition is possible. The sfg derivations necessary to do this are shown in consecutive steps in Fig. 4. These are the main contributions of this paper. The steps in Fig. 4(d)–(h) are typical sfg transformations i.e., node splitting, shifting a transmittance (shifting the termination point of an internal branch), and loop reduction (e.g. see [8] and [9]). In Fig. 4(i) a sfg with only negative integrator paths and adders having some incoming branches with negative gain is obtained. However, the corresponding active circuit would have some passive negative components. To eliminate these, additional nodes have to be multiplied by $-1$ as shown in Fig. 4(j)–(l), resulting in positive and negative integrators, and all-positive incoming branches. The final filter is shown in Fig. 5. Capacitor values readily follow from (6), whereas resistor values are simply calculated as reciprocals of path transmission values in (7); both capacitor and resistor values are shown in Fig. 5 in normalized form.
Figure 4. Deriving an active-RC simulation of a seventh-order passive-LCR ladder filter. (a) Initial graph (repeated graph from Fig. 1(b)). (b)–(c) Producing all voltage nodes; multiplication of current nodes by $R_0$. The reduction rules that apply follow: (d) Shifting the termination point of internal branches $C_2/C_3'$ (the same is done with branches $C_4/C_5'$ and $C_6/C_7'$). (e) Shifting the termination point of internal branches $C_2/C_1'$ (and of $C_4/C_3'$ and $C_6/C_5'$ in the same way). The result of (d) and (e) is in (f). (g) Removal of self-loops and reduction of parallel branches. (h) Shifting the termination point of branches $C_2C_4(C_1''C_3')$, $C_6C_4(C_3''C_5')$, and $C_6C_4(C_1''C_5')$. (i) Removal of self-loops and reduction of parallel branches. (j)–(l) Multiply appropriate nodes by $-1$ in order to obtain only positive components with positive and negative integrators.

Capacitors in Fig. 4(i) are calculated from [use also (4)]:

$$C_1'' = C_1\left(1 - \frac{C_2}{C_1'C_3'}\right), C_3'' = C_1\left(1 - \frac{C_2}{C_1'C_3'} - \frac{C_2}{C_1'C_5}\right),$$

$$C_5'' = C_5\left(1 - \frac{C_2}{C_3'C_5} - \frac{C_2}{C_5'C_7}\right), C_7'' = C_7\left(1 - \frac{C_2}{C_3'C_7}\right).$$

$$C_1''' = C_1\left(\frac{C_2'C_4}{C_1'C_3'C_5}\right), C_3''' = C_3\left(1 - \frac{C_2'C_4}{C_3'C_5'C_7}\right),$$

$$C_5''' = C_5\left(1 - \frac{C_2'C_6}{C_3'C_5'C_7}\right), C_7''' = C_7\left(1 - \frac{C_2'C_6}{C_5'C_7}\right).$$

(6)
Figure 5. Final seventh-order active-RC ladder filter simulation with minimum capacitors (sfg is in Fig. 4(l)).

The conventional realization of the filter, with a capacitive network realizing the three tank capacitors as presented in Fig. 3, is not new (see [6] and [7]). The branches realizing the tank capacitors are obtained in the same way for all filter orders. On the other hand, the realization of finite zeros with resistive networks as presented in Fig. 5 is new, and requires a complicated sfg transformation leading to additional signal paths. Note also that new circuit has more opamps and resistors than the conventional one. This difference in complexity, i.e. in total number of passive and active components (but with canonic number of capacitors), increase with increasing order. In the latter circuit, large resistors such as $R_{20}$–$R_{31}$ can be replaced by resistive T-networks with small values as shown in [1].

III. SENSITIVITY ANALYSIS

In what follows, we examine the sensitivity to tolerances of passive component values of the original elliptic passive-LCR CC 07 25 50 filter whose amplitude characteristics are shown in Fig. 6(a) with that of the two active, simulated filters discussed above. Using the OrCAD PSpice 16 program [3] with Monte Carlo runs, we assume a zero-mean uniform distribution, and a 5%
standard deviation for all components. The obtained spread of responses for each filter is an indication of that filter's sensitivity to component tolerances. It is also an indication of the number of components in a given circuit; the fewer this number, the smaller will be the spread of responses resulting from the accumulated component tolerances.

The sensitivity of the passive-LCR filter (see Fig. 1(a)) is shown in Fig. 6(b). That of the active-RC simulation with a capacitive network (see Fig. 3) is shown in Fig. 6(c), and that of the active-RC simulation with a resistive network (see Fig. 5) in Fig. 6(d). Both active-RC filters have similarly low sensitivity, but larger sensitivity than the original passive-LCR filter (Fig. 6(b)). This is because they contain a larger number of components. As expected from Orchard's theorem [2], all three filters have low sensitivity in the pass band.

In this paper (as well as in [1]) the main contribution has been the derivation of low-sensitivity elliptic filters having canonic number of capacitors. Therefore, in all simulations using PSpice instead of real opamp models, ideal voltage-controlled-voltage sources (VCVS) denoted by “E” with frequency-independent gain set to $10^6$ have been used.

IV. CONCLUSION

In this paper (and in the companion paper [1]) we compare two realizations of active-RC elliptic ladder filters which are the inductorless equivalent of a given passive-LCR ladder filter. One is classical and well known; it features an additional capacitive network that realizes the series capacitors required to form parallel tanks. The second, which is new, uses additional resistive networks to replace the additional series capacitors of the first circuit. This reduces the total number of capacitors in the circuit. This reduction increases with the filter order.

In this paper it is shown that the realization of the newly proposed circuit becomes more complicated when the order is increased in terms of the increasing complexity of the sfg transformation. Consequently, the additional resistive network also becomes more complicated (see also [1]).

The sensitivity of the two circuits is compared, and it is concluded that no noticeable difference exists between them. Nevertheless, since the resistive network saves capacitors (which are generally more difficult to manufacture especially on-chip), the elliptic filter, with a resistive network for the realization of finite zeros, may be a very useful alternative to the conventional circuit.

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REFERENCES